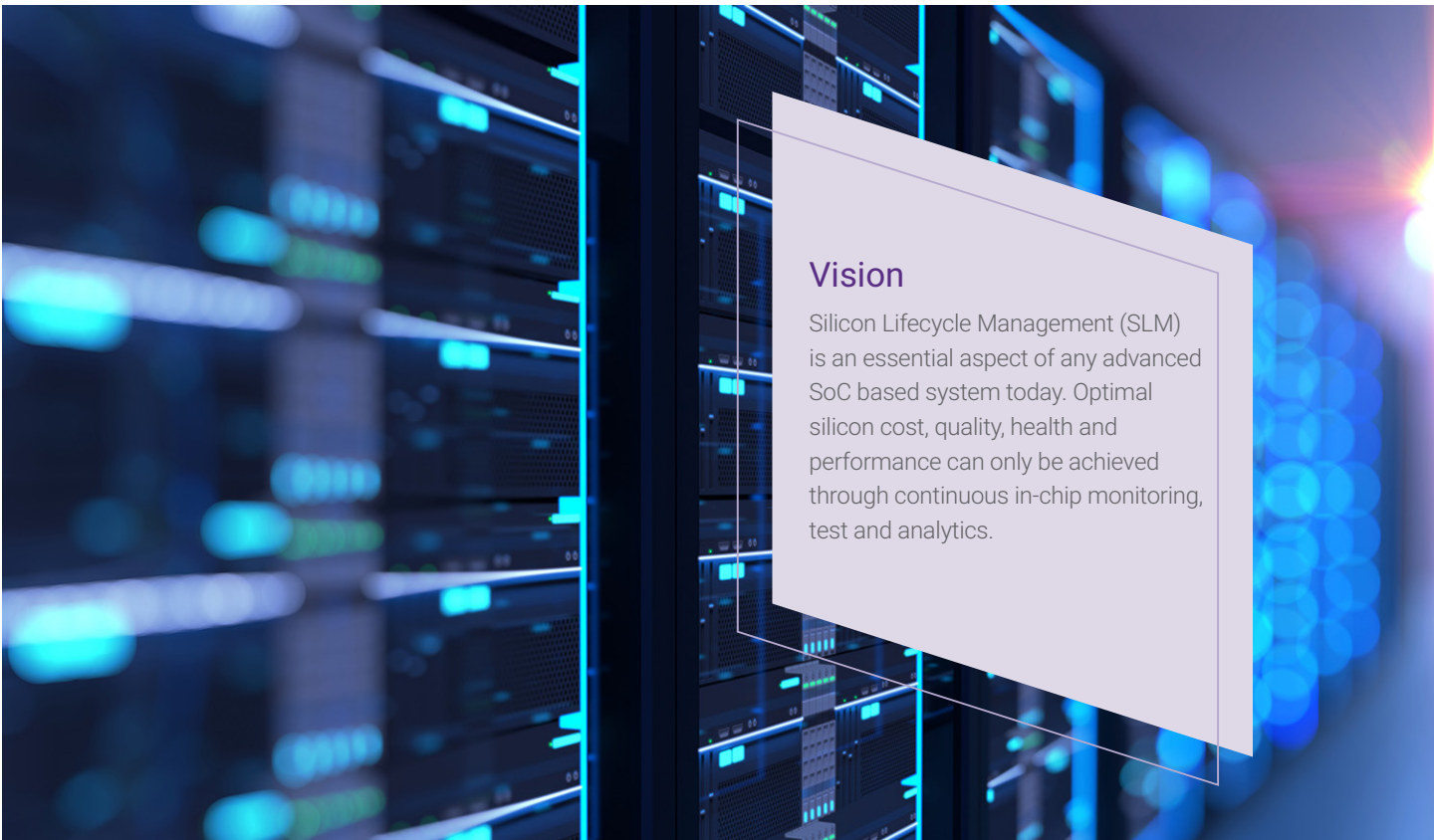


Silicon Lifecycle Management Family

Improving silicon health and operational metrics
at each phase of the system lifecycle





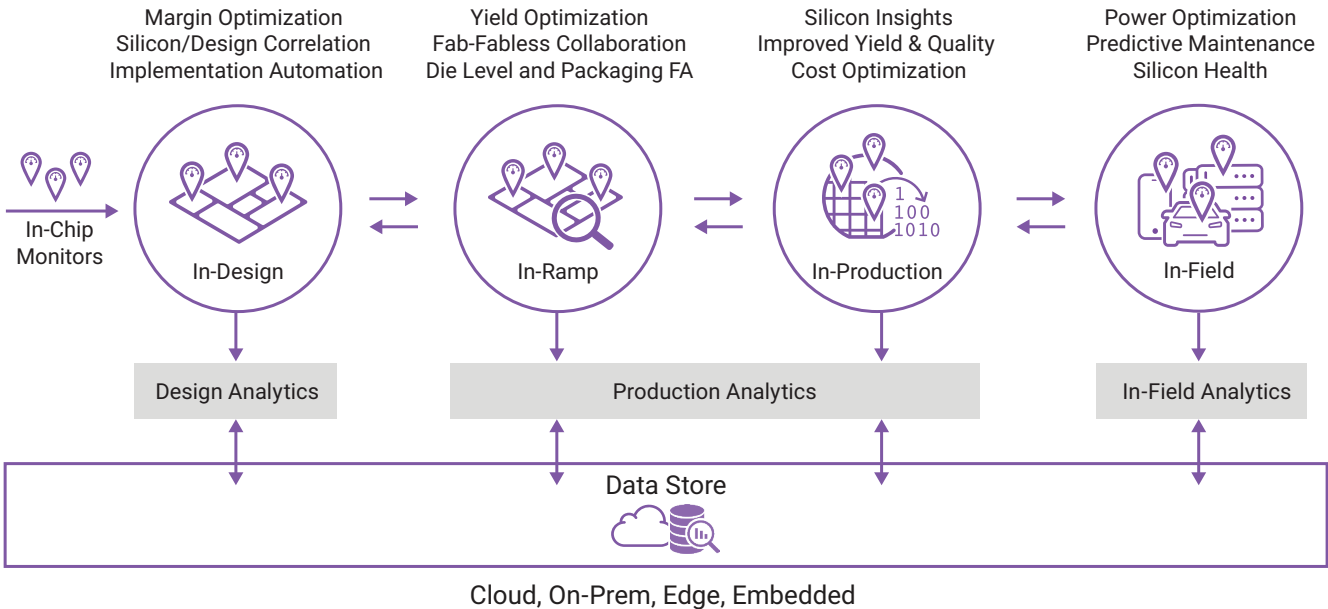
Vision

Silicon Lifecycle Management (SLM) is an essential aspect of any advanced SoC based system today. Optimal silicon cost, quality, health and performance can only be achieved through continuous in-chip monitoring, test and analytics.

Synopsys SLM Family

The Synopsys SLM family is designed to improve silicon health and operational metrics at every phase of the system lifecycle. SLM is built on a foundation of in-chip IP, data analytics and design automation. Environmental, structural and functional monitors enable deep insights from SoC manufacturing to In-Field systems. Meaningful data is gathered at every opportunity for continuous analysis and actionable feedback. SLM fully leverages Synopsys' solutions for design automation.

Actionable Insights Through Silicon Lifecycle Monitoring and Analytics



SLM IP

The Synopsys SLM Family is built on a foundation of monitor IP. There are three classifications of IP: Environmental, Structural and Functional monitors. Each gather relevant data throughout the silicon lifecycle of the device. Environmental monitors optimize silicon performance based on the operating environment. Structural monitors provide data on silicon performance variation from design to in-field. Functional monitors report on the health of critical functions of the device.

PVT Monitors

Process, Voltage and Temperature (PVT) monitoring is critical for optimal operation and performance in today's SoCs

- Maximizes performance, power, reliability
- Highly accurate, distributed monitoring throughout the die
- Available on process nodes from 28nm to 3nm

Path Margin Monitors

Measure timing margin of actual functional paths in-test and in-field

- Monitor 1000+ synthetic and functional paths
- Optimize silicon performance based on actual margins available
- Automated path selection, IP insertion, and scan generation

Clock and Delay Monitors

Measure delay between edges of a signal(s)

- Clock duty cycle quality check
- Memory access time tracking with BIST
- Digital delay line test characterization

UCle Monitor, Test & Repair

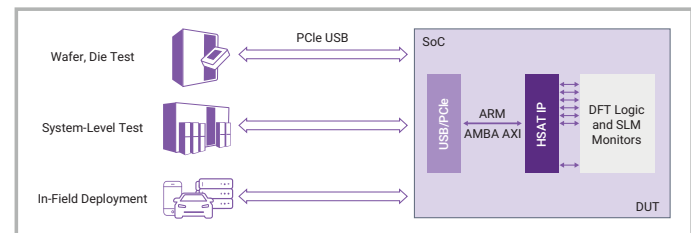
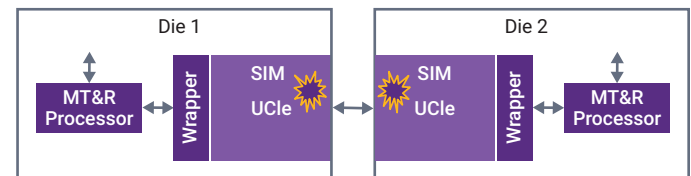
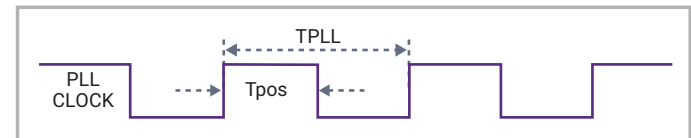
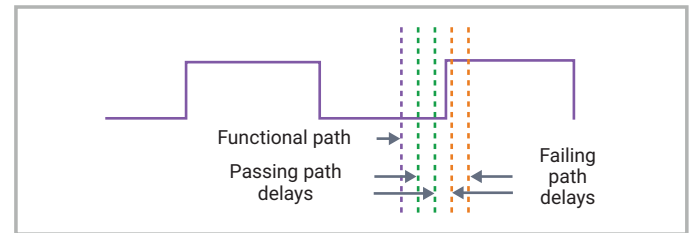
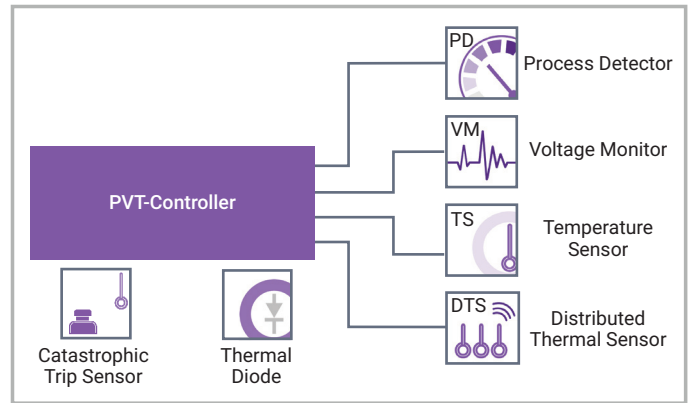
Comprehensive UCle SLM solution

- Monitor signal quality on D2D UCle lane(s)
- Logic BIST with near and far end modes
- Repair lanes with redundancy allocation In-Field

High Speed Access & Test

Enable testing over functional interface (PCIe, USB, SPI, ...)

- Used during In-Field operation as well as WS, FT, SLT
- Supported by instruments from leading ATE providers
- Reduced pin count & test hardware saves cost



SMS

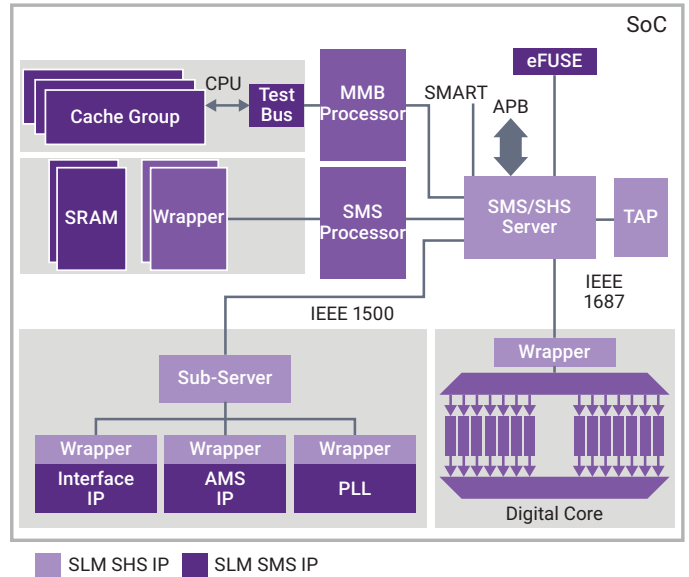
Comprehensive silicon proven test, repair and diagnostics solution

- Supports Synopsys and 3rd party SRAM/RF/ROM, CAM, eMRAM and DRAM
- High Performance core support
- FinFET specific memory test algorithm programmability

SHS

Automated hierarchical test solution for SoC's

- Automated hierarchical test
- Automated test integration of all IP/cores with in-syste scheduling
- Pre-validated ready ATE patterns with pattern porting



SLM Design and Production Analytics

Avalon is a next-generation CAD navigation and fault isolation software tool for failure analysis, design debug and low-yield analysis. It provides a complete solution for fast, efficient, and accurate investigation of inspection, test and failure analysis jobs.

SysNav extends Avalon's die level failure analysis to the package, offering a multi-chip module (MCM) and printed circuit board (PCB) layout viewer with interactive signal tracing and cross-mapping between board and die for defect analysis and product debug.

Silicon.da is a unified analytics solution that covers all product manufacturing phases, and provides the ability to analyze petabytes of silicon and system data. It automatically highlights silicon data outliers, enabling engineering teams to quickly identify and correct underlying issues in the semiconductor supply chain.

With Silicon.da, engineering teams can leverage silicon design, monitor, diagnostic, fab and production test data to improve key chip production metrics such as quality, yield and throughput, as well as key silicon operational metrics such as chip power and performance.

Silicon.da provides key benefits in the area of Engineering Productivity, Silicon Efficiency, and Tool Scalability.



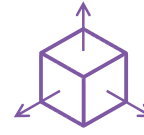
Productivity

- Actionable insights out-of-the-box
- Automated root cause analysis
- Accurate FA candidate selection



Efficiency

- Power and performance optimization
- Quality, yield, throughput optimization
- Real-time production control



Scalability

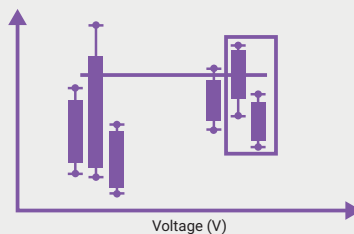
- Petabytes of data
- Multi domain support
- Cloud enabled

Silicon Model Calibration



Improved design optimization flow

Process Classification



Accurate binning & debug

V_{min} Prediction



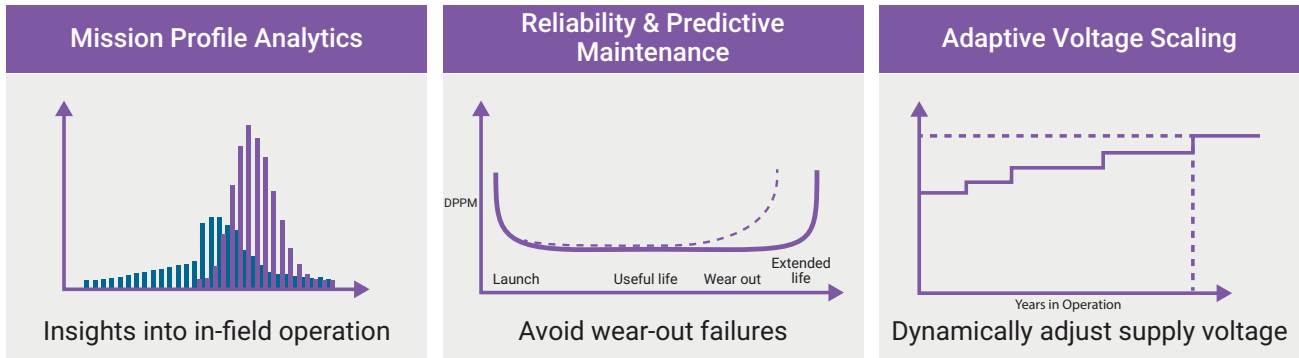
Monitor driven V_{min} Prediction

SLM In-Field Analytics

Once a device is deployed into the field it is essential that it is continually monitored, tested, analyzed and potentially adapted. On-chip or cloud-based analytics can be used for predictive maintenance, aging identification, and fault detection in order to mitigate the risk of catastrophic system failures.

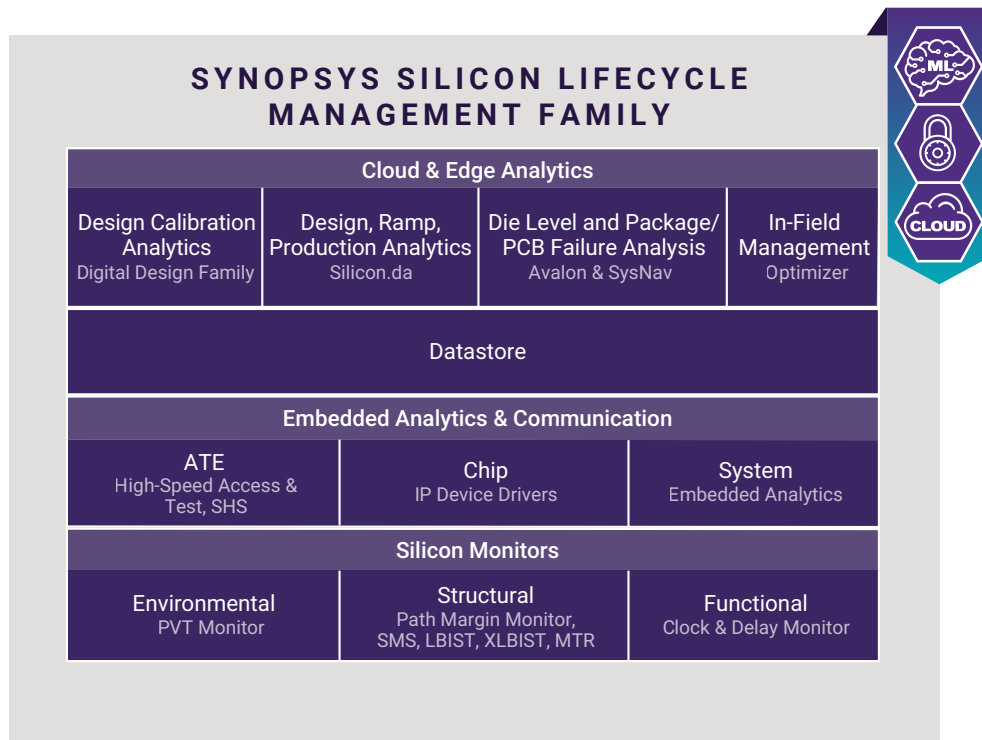
Monitor data can also enable real-time analytics and optimization schemes, such as Adaptive Voltage Scaling (AVS) resulting in lower power and extend device lifetime.

Finally, cloud-based analysis of data from design, manufacturing and in-field provides powerful insights into the health of a fleet of devices, enabling better informed decisions to address root cause analysis for traceability and RMAs.

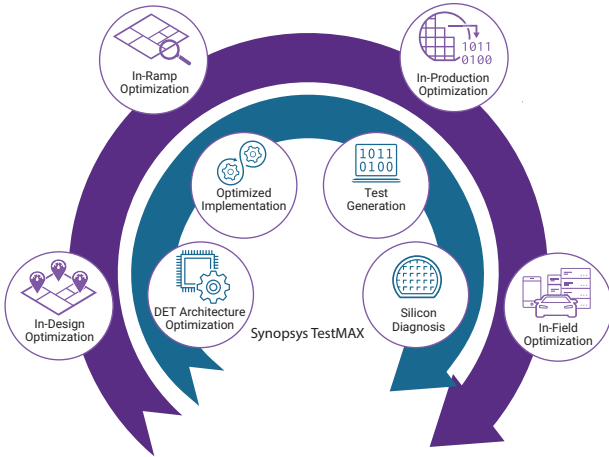


SLM Established Tool Solutions

The Synopsys Silicon Lifecycle Management Family includes multiple integrated products and capabilities. The key components of SLM are highlighted below:



Synopsys SLM



SLM & Test Synergy

Synopsys SLM and Synopsys TestMAX™ solutions encompass integrated tools, IP and methodologies to test, monitor and analyze SoCs, providing actionable insights at every phase of the device lifecycle.

These innovative test and analytics tools enable a unified flow that is securely connected to Synopsys' Fusion Design Platform for deep insights, from in-design to in-field, meeting design, test, and operational goals concurrently for the entire lifespan of a silicon device.

For additional information on Synopsys Silicon Lifecycle Management and Synopsys TestMAX solutions, please visit our website or contact us.