SYNOPSYS®

DATASHEET

TestMAX Vtran

Advanced Vector Translation

Reads and reformats patterns and results for over 30 ATE and logic simulator formats

Overview

Synopsys TestMAX Vtran® is a vector translation program that reads patterns and results from TestMAX ATPG, Synopsys VCS® simulator, and third-party automatic tools, then re-formats them for more than 30 popular automated test equipment (ATE) and logic simulator formats. ATE patterns can be easily validated reading back the ATE patterns back into TestMAX Vtran, which then creates a Verilog testbench for verification. For ease-of-use, a graphical TestMAX Vtran contains a user interface and creates a waveform database for Synopsys Verdi debugger.

Key Benefits

- Enables portability of ATPG and simulation patterns across multiple ATEs
- Reduces turn-around-time with creation of validation testbenches
- Easily view and debug waveforms of ATPG and ATE formatted patterns

Features

- Translates ATPG patterns and simulation change dump values into various ATE formats and Verilog simulators
- Creates testbenches for Verilog simulation-based verification
- Reformats simulation data files generated by one simulator into files compatible with another simulator
- Enables modification of simulation data such as pin lists, pin order, bus radixes, time offsets, pin timing and time scaling
- Contains a user interface for various format options
- Processes ATPG and ATE files for viewing the corresponding waveforms using Synopsys Verdi

ATPG, Simulator, and ATE Formats

TestMAX Vtran reads from multiple sources and supports the most popular formats. For an exact list, please contact your local Synopsys account team. Popular file formats include:

- WGL and IEEE 1450 (STIL) [Compatibility tested with TestMAX ATPG]
- Verilog eVCD and VCD (value change dump)
- Leading ATE vendor formats including: Advantest, Teradyne, LTX-Credence

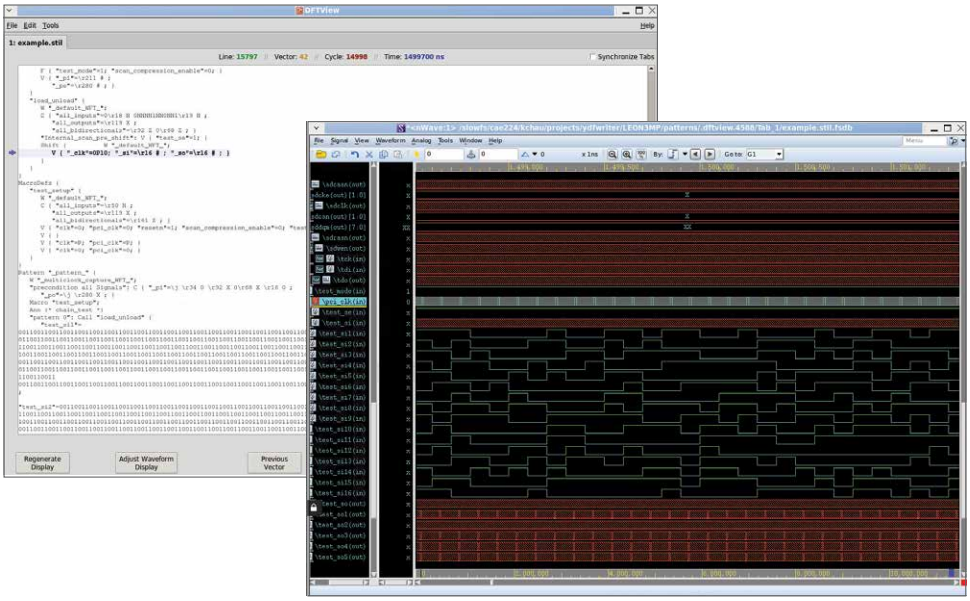

Figure 1: View of waveforms generated by TestMAX Vtran

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