SYNOPSYS®

DATASHEET

VCS AMS

Mixed-Signal Verification Solution

Scalable mixed-signal regression testing with transistor-level accuracy

Overview

The complexity of mixed-signal system-on-chip (SoC) designs is rapidly increasing due to growing analog content, advanced analog and digital interfaces and tougher requirements for safety and reliability. This is driving a crucial need for advanced verification methodologies and technologies. Synopsys' VCS® AMS mixed-signal verification solution, incorporating VCS functional verification and the CustomSim™ FastSPICE simulator, delivers advanced functional and low-power verification technologies combined with class-leading performance and capacity for faster mixed-signal SoC regression testing.

Introduction

The VCS AMS mixed-signal verification solution delivers class-leading performance and capacity for faster mixed-signal SoC regression testing. By natively integrating advanced technologies for functional and low-power verification, coupled with analog extensions to the proven UVM methodology, VCS AMS enables the rapid development of a coverage-driven, constrained-random testbench that can be run in parallel across compute farms to reduce overall regression testing cost.

Figure 1: VCS AMS

Performance

VCS AMS benefits from a proprietary integration of high performance analog and digital simulation engines. While other mixed-signal verification solutions lag in performance due to their slow analog simulation engine and have to rely on behavioral modeling for improvement, VCS AMS integrates CustomSim's FastSPICE engine to provide class-leading performance with transistor-level accuracy.

Multicore Technology

By supporting multicore simulation technology in its FastSPICE engine, VCS AMS delivers even higher verification throughput, enabling scalable mixed-signal regression testing with transistor-level accuracy (see Figure 2).

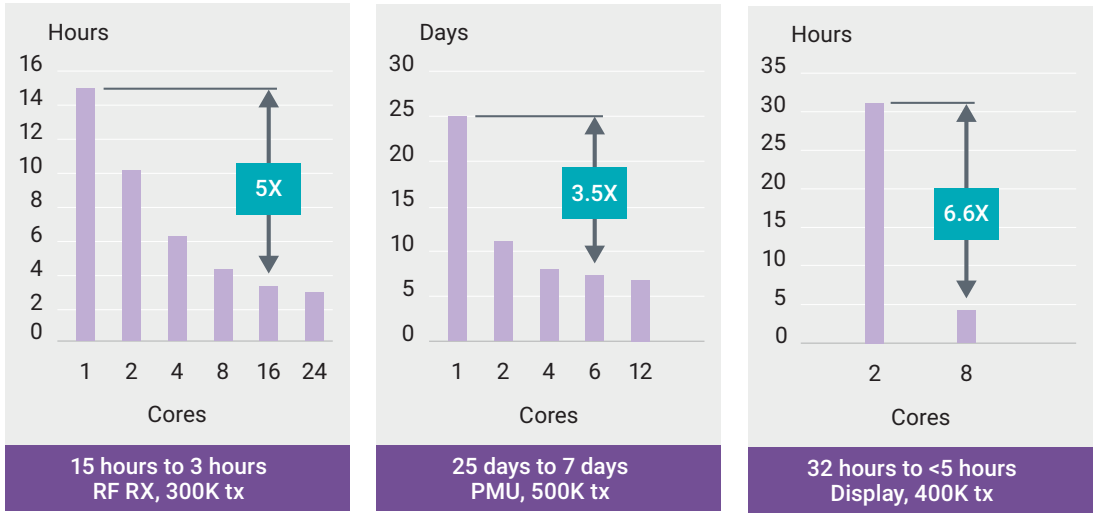

Figure 2: VCS AMS multicore performance improvement examples

Flexibility

As different mixed-signal design applications require different configurations of SPICE netlist, RTL and behavioral models, flexibility in languages and topologies supported is crucial for a mixed-signal verification solution. As more or less accuracy may be needed as the design and verification process progress, the solution should be configurable between SPICE-level representation to more abstract levels, such as Verilog-AMS or Real Number Modeling. VCS AMS offers a versatile use model enabling any mixture of abstraction level and design hierarchy with language support for SystemVerilog, Verilog, VHDL, Verilog-AMS and SPICE (see Table 1). Post-layout simulation is supported through SPF, DSPF and SPEF formats.

Analog	Digital	Mixed-signal
SPICE	Verilog	Verilog-AMS
Verilog-A	VHDL	Real number model
SPEF, DSPF, DPF	SystemVerilog	
	SystemC, Matlab	

Table 1: Modeling languages and formats supported by VCS AMS

VCS AMS fully enables complex design architectures by providing not only analog, digital or mixed-signal on top configurations, but also any number of hierarchy levels for those configurations.

Increased Productivity

Achieving time-to-market goals is a critical driver for today's mixed-signal SoC designs. Ease-of-use and early detection of design errors caused by complex inter-block connectivity or analog-to-digital interfaces are key requirements of a productive mixed-signal verification solution. VCS AMS offers the following features to minimize setup time, identify connectivity errors and increase verification productivity:

- **Easy setup:** mixed-signal configuration and setup are minimal due to netlist-driven flow support
- **Automatic insertion of analog-to-digital interface elements:** the correct interface elements are automatically inserted with parameter optimization (direction, voltage supply, impedance, strength) to avoid convergence or accuracy issues
- **Diagnostic reports:** reports are automatically generated on interface elements, connectivity, port mapping and design hierarchy to enable debug of design connectivity errors during simulation
- **Save and restore:** enables faster regression testing throughput by resuming simulation from a previously saved state

Native Circuit Checking for Power Management

Many SoC design failures happen at the mixed-signal interface so verifying that electric design rules are not violated and power domains are not mismatched is crucial at the chip level. VCS AMS provides a comprehensive set of static and dynamic native checks to quickly identify electric rule violations and power management design errors (see Figure 3). With this technology, mixed-signal designers can identify violations such as missing level shifters, leakage paths or power-up checks at the SoC level and avoid design errors before tapeout.

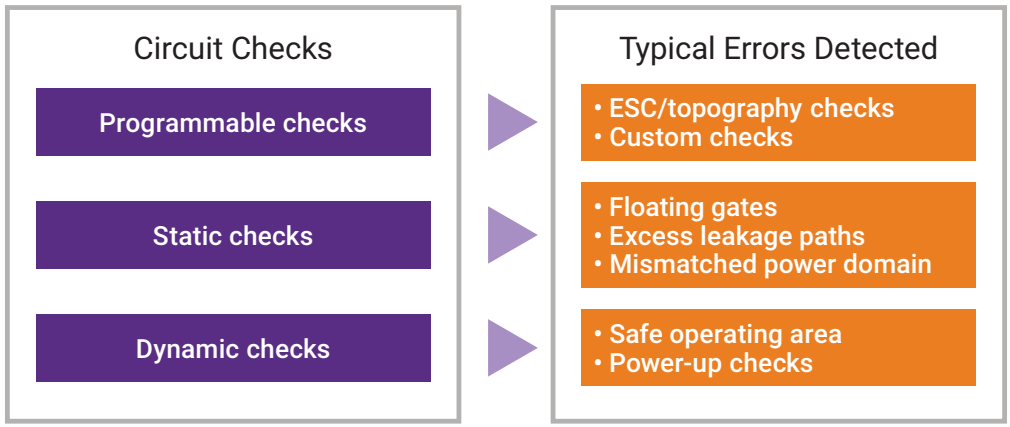

Figure 3: VCS AMS native circuit checks enable ERC and low-power diagnostics

Low-power Verification

VCS AMS provides a comprehensive mixed-signal low-power verification solution by extending VCS native low power (NLP) technology, supporting UPF, for mixed-signal designs. While passing voltage levels between digital and analog, interface elements are automatically inserted to accurately model power design intent (see Figure 4). This approach automates a tedious and error-prone process and provides a system-level solution for low power.

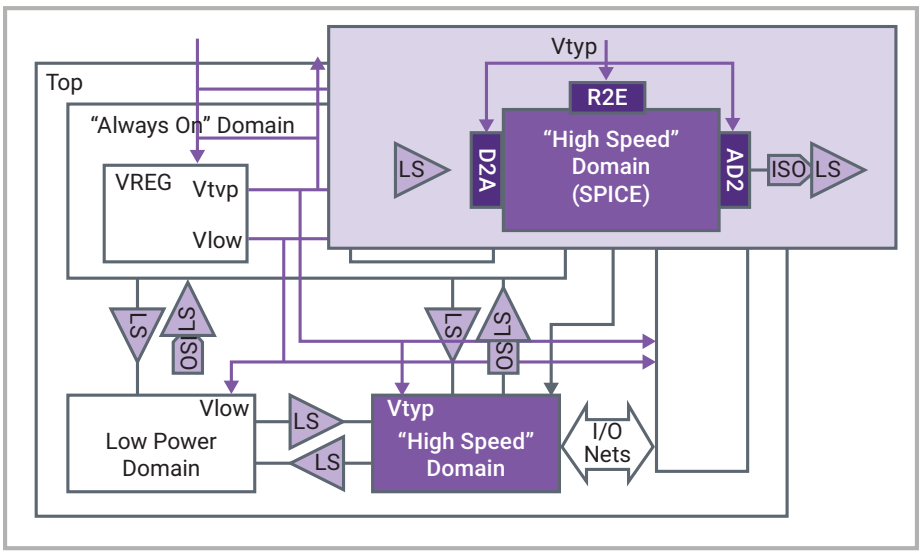

Figure 4: VCS AMS extends NLP to mixed-signal by passing the right power level and adjusting interface elements accordingly

Advanced Mixed-signal Behavioral Modeling

VCS AMS provides a broad solution for advanced behavioral modeling by providing support for Verilog-AMS and real number modeling (real, wreal and SystemVerilog nettype). Verilog-AMS was the first language introduced in the mixed-signal space and aimed to provide a good trade-off between accuracy and speed. This language has however several limitations that made its adoption really challenging, especially for modern SoCs: incorrect modeling leading to convergence issues or poor performance, necessity for calibration of those models versus their SPICE counterparts.

Real number modeling (real, wreal) represents the second generation of behavioral modeling. It models the analog behavior in the digital domain using discretely simulated REAL values. The end result is a considerable speed-up in simulation, but with less accuracy. In addition, real number modeling has some existing language limitations: lack of support for user-defined types that can hold one or more real and user-defined resolution functions, and no true relationship between current and voltage.

To alleviate the limitations in current behavioral modeling approaches (see Figure 5), VCS AMS introduces the next generation of real number models based on SystemVerilog.

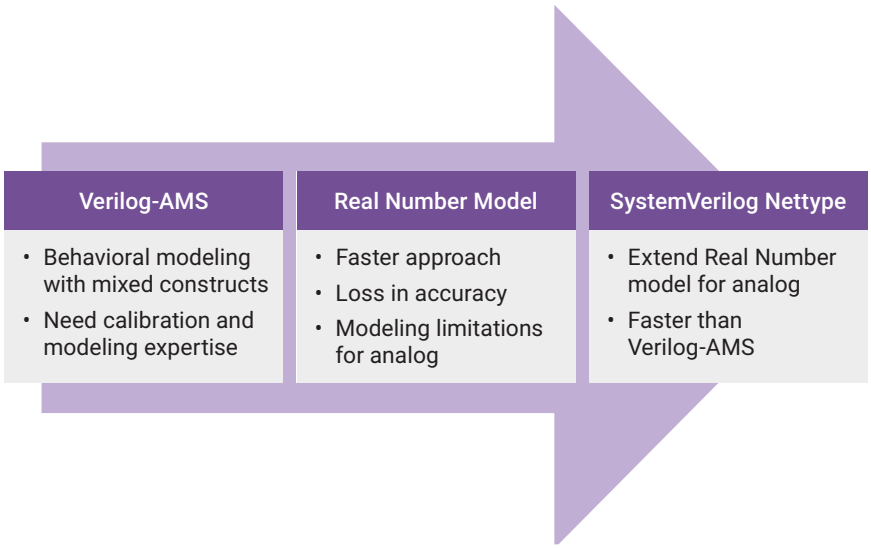

Figure 5: Verilog-AMS and real number modeling leading to SystemVerilog nettype

SystemVerilog nettype provides significant modeling improvements for modern mixed-signal SoC verification:

- User-defined types that can hold one or more real values
- User-defined resolution functions
- Dynamic selection of an interconnect type based on connectivity
- Modeling flexibility

SystemVerilog nettype provides high performance and broad modeling capabilities for faster verification with higher accuracy.

AMS Testbench

Synopsys' AMS Testbench extends the proven SystemVerilog-based UVM methodology, equipping mixed-signal designers to:

- Integrate reference models with various abstraction levels
- Introduce assertions and checkers on analog nodes
- Sample analog nodes to monitor incoming traffic
- Introduce constraint-random verification for driving analog nodes
- Introduce analog coverage
- Introduce verification planning and regression management in a mixed-signal context

Using AMS Testbench, verification techniques that are standard practice in digital verification can be leveraged to rapidly develop a powerful constrained-random, coverage-driven testbench for regression testing of mixed-signal SoCs (see Figure 6).

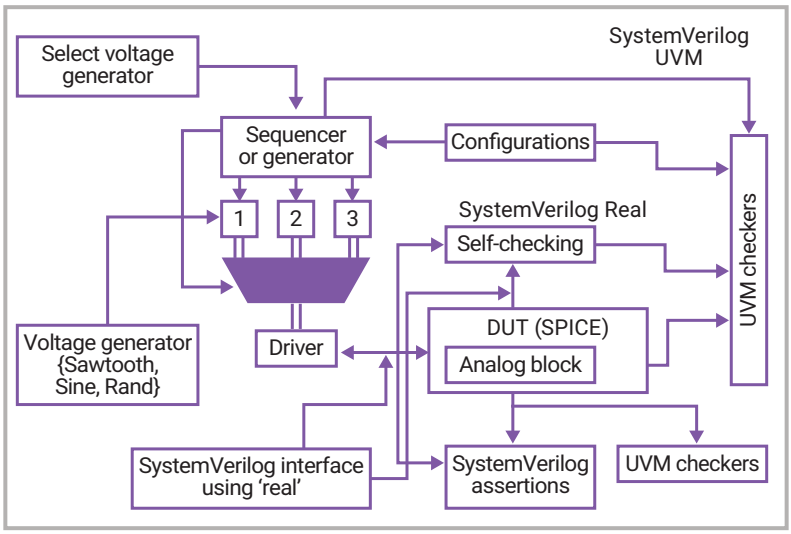

Figure 6: AMS Testbench for analog IP

Debug Environment

VCS AMS is supported by Synopsys debug environments (see Figure 7). Synopsys' custom Simulation and Analysis Environment (SAE) provides a schematic-based solution, while the Discovery™ Visualization Environment (DVE) and Verdi® Advanced AMS Debug offer advanced debug and visualization environments supporting a rich set of verification features including:

- Low power
- SystemVerilog testbench debug
- Coverage reporting and visualization
- Verification planning and management

TCL support is provided for interaction or batch control and menu customizations across SAE, DVE and Verdi.

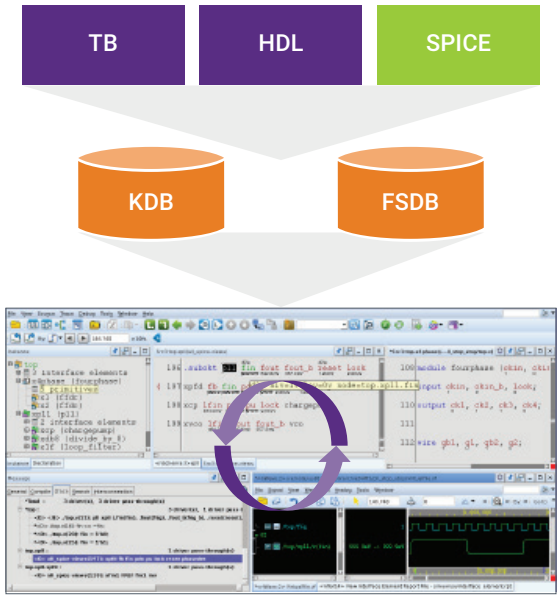

Figure 7: Verdi Advanced AMS Debug

Inputs supported

- HSPICE®, Spectre & Eldo netlist formats
- SystemVerilog, Verilog, VHDL
- SystemC
- Common HSPICE device models, Spectre & Eldo models
- Verilog-A, Verilog-AMS and Real Number modeling
- SPEF, DPSF and SPF for post-layout parasitic data
- VCD and VEC stimulus input format
- TCL scripting

Outputs supported

- FSDB, VPD, WDF, WDB for analog waveform database formats
- FSDB, VPD for digital waveform database format
- VPD for unified analog/digital waveform database format

Platforms supported

- SPARC Solaris
- x86 Red Hat Enterprise
- x86 SUSE Enterprise

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